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8296/8297 GPIO BUS TRANSCEIVER

- Octal Open-Collector or Three-State GPIO Line Drivers
- Octal Schmitt-Type Line Receivers
- Low-Power HMOS II Design
- Power Up/Power Down Protection to Prevent Disrupting the Bus
- Two 20-Pin Transceivers Connect 8291 Directly to GPIO Bus Including On-Chip IEEE-488 Bus Terminations
- Only 8291, 8296, and 8297 Required to Form Complete IEEE-488 Talker/Listener Interface with No Additional Components

The Intel® 8296/8297 GPIO Bus Transceivers are high-current, non-inverting buffer chips designed to interface the 8291 GPIO Talker/Listener to the IEEE Standard 488-1978 Instrumentation Interface Bus. The 8296 and 8297 are optimized to simplify a talker/listener configuration so that the 8291 can be connected to the GPIO bus without any external hardware. The 8297 connects the five IEEE-488 control lines and three handshake lines to the 8291 with a special output for parallel poll. The 8296 connects the eight data lines to the 8291, or it can be used as a general purpose high-current bus transceiver.

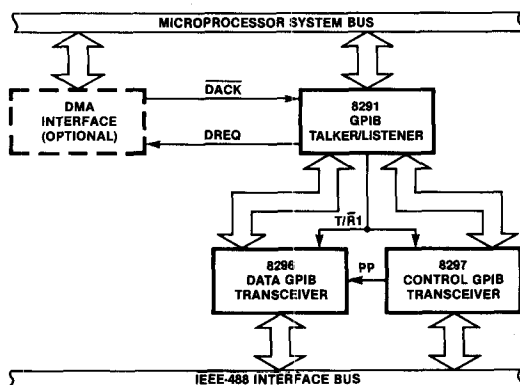


Figure 1. 8291, 8296, 8297 System Diagram

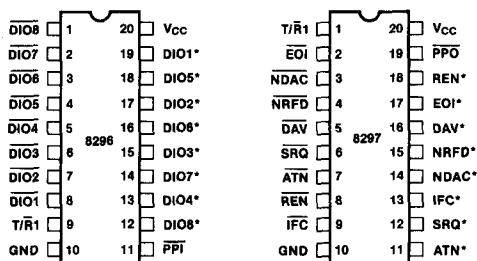


Figure 2. Pin Configuration

Table 2. 8297 Pin Description

Symbol	Pin No.	Type	Name and Function
$\overline{T/R1}$	1	I	Transmit/Receive 1: Direction control for NDAC, NRFD, and DAV. \overline{EOI}^* is gated by \overline{ATN}^* and $\overline{T/R1}$ so that it will remain an input during a parallel poll. If $\overline{T/R1}$ is high, then \overline{NDAC}^* and \overline{NRFD}^* are inputs while \overline{DAV}^* and \overline{EOI}^* (if \overline{ATN}^* is high) are outputs. This input is TTL compatible.
\overline{EOI}	2	I/O	End or Identify: Processor GPIB control line; used by a talker to indicate the end of a multiple byte transfer. This pin is TTL compatible.
\overline{NDAC}	3	I/O	Not Data Accepted: Processor GPIB handshake line; used to indicate the data has been accepted by all listeners. This pin is TTL compatible.
\overline{NRFD}	4	I/O	Not Ready For Data: Processor GPIB handshake line; used to indicate the listener is ready to accept another byte. This pin is TTL compatible.
\overline{DAV}	5	I/O	Data Available: Processor GPIB handshake line; used to indicate the talker has inserted data onto the bus. This pin is TTL compatible.
\overline{SRQ}	6	I	Service Request: Processor GPIB control line; used to indicate the need for service. This input is TTL compatible.
\overline{ATN}	7	O	Attention: Processor GPIB control line; used to determine whether the byte being received is data or control. This output is TTL compatible.
\overline{REN}	8	O	Remote Enable: Processor GPIB control line; used to select between remote or local device programming. This output is TTL compatible.
\overline{IFC}	9	O	Interface Clear: Processor GPIB control line; used to reset the interface. This output is TTL compatible.
GND	10	PS	Circuit Ground Potential.

Symbol	Pin No.	Type	Name and Function
V_{CC}	20	PS	Positive Power Supply: (5V \pm 10%).
\overline{PPO}	19	O	Parallel Poll Out: Signal to the 8296 to indicate a parallel poll is being performed (both \overline{ATN}^* and \overline{EOI}^* are low).
\overline{REN}^*	18	I	Remote Enable: IEEE-488 GPIB control line; this input is an IEEE-488 compatible Schmitt trigger.
\overline{EOI}^*	17	I/O	End or Identify: IEEE-488 GPIB control line; used by a talker to indicate the end of a message, and by the controller with \overline{ATN}^* to indicate a parallel poll. It is an input whenever \overline{ATN}^* is low or $\overline{T/R1}$ is low. This pin is IEEE-488 compatible for input and output.
\overline{DAV}^*	16	I/O	Data Available: IEEE-488 GPIB handshake line; is a GPIB driver when $\overline{T/R1}$ is high and is push-pull except during a parallel poll. This pin is IEEE-488 compatible for input and output.
\overline{NRFD}^*	15	I/O	Not Ready For Data: IEEE-488 GPIB handshake line; is an open-collector GPIB driver when $\overline{T/R1}$ is low. This pin is IEEE-488 compatible for input and output.
\overline{NDAC}^*	14	I/O	Not Data Accepted: IEEE-488 GPIB handshake line; is an open-collector GPIB driver when $\overline{T/R1}$ is low. This pin is IEEE-488 compatible for input and output.
\overline{IFC}^*	13	I	Interface Clear: IEEE-488 GPIB control line; this input is an IEEE-488 compatible Schmitt trigger.
\overline{SRQ}^*	12	O	Service Request: IEEE-488 GPIB control line; this output is an open-collector IEEE-488 compatible driver.
\overline{ATN}^*	11	I	Attention: IEEE-488 GPIB control line; this input is an IEEE-488 compatible Schmitt trigger.

Table 1. 8296 Pin Description

Symbol	Pin No.	Type	Name and Function
$\overline{\text{DIO8}}$ – DIO1	1–8	I/O	Data Input/Output: Processor GPIB data lines; used to carry message and data bytes in a bit-parallel byte-serial form. If $\text{T}/\overline{\text{R1}}$ is high, these lines are inputs. These lines are TTL compatible.
$\text{T}/\overline{\text{R1}}$	9	I	Transmit/Receive 1: Controls the direction of the DIO lines. If $\text{T}/\overline{\text{R1}}$ is high, then the eight DIO lines are driving data onto the IEEE-488 bus. This input is TTL compatible.
GND	10	PS	Circuit Ground Potential.

Symbol	Pin No.	Type	Name and Function
V_{CC}	20	PS	Positive Power Supply: (5V $\pm 10\%$).
DIO1^* – DIO8^*	19, 17, 15, 13, 18, 16, 14, 12	I/O	Data Input/Output: IEEE-488 GPIB data lines. They are IEEE-488 compatible Schmitt triggers when used for input and can sink over 48 mA when used for output. If $\text{T}/\overline{\text{R1}}$ is high, these lines are driving the bus. If PPI is high, then these lines are open-collector for a parallel poll; otherwise, they are push-pull line drivers. These pins are IEEE-488 compatible for input and output.
$\overline{\text{PPI}}$	11	I	Parallel Poll In: Input from the 8297 which indicates whether or not a parallel poll is being conducted. The 8296 is a push-pull (three-state) driver for data bytes, but it becomes an open-collector driver for a parallel poll.

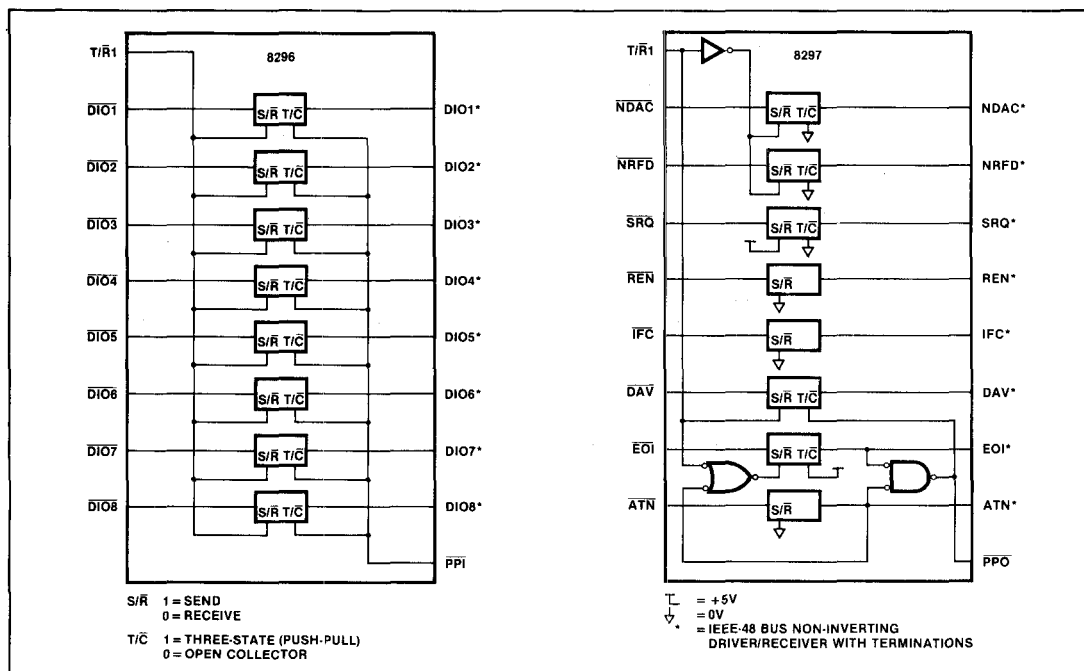
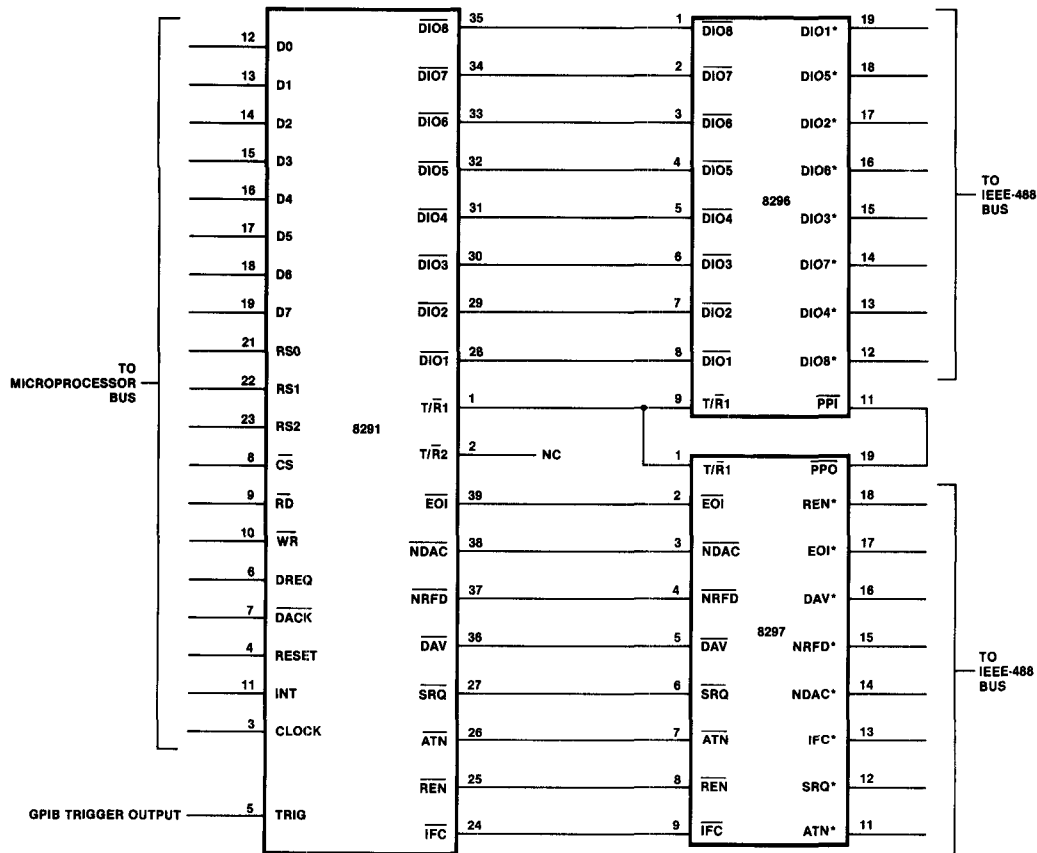


Figure 3. 8296/8297 Transceiver Control Configuration



* = IEEE-488 COMPATIBLE GPIB NON-INVERTING TRANSCEIVER.

Figure 4. 8291, 8296, 8297 System Configuration